Computación y Sistemas Vol. 9 Núm. 2, pp. 119-132

Computing Symbolic Expressions in Analog Circuits Using Nullors

Cálculo de Expresiones Simbólicas en Circuitos Analógicos usando Anuladores

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Article received on July 14, 2003; accepted en July 08, 2005

Abstract

A novel method is introduced to compute symbolic expressions in analog circuits modeled by nullors. The proposed method is based on the formulation of a compact system of equations (CSEs) by manipulation of data-structures, which highly improves traditional symbolic-methods. It is demonstrated that by modeling all active devices using nullors, the CSEs is easily formulated by manipulation of both the nullor and admittance interconnection-relationships. Several examples leads us to conclude on the suitability of the proposed symbolic-method to be incorporated within a symbolic simulator.
Keywords: Symbolic analysis, Modeling and simulation, Circuit theory, Data structures, Nullor.

Resumen

Se presenta un nuevo método para calcular expresiones simbólicas en circuitos analógicos modelados con anuladores (nullors). El método propuesto se basa en la formulación de un sistema de ecuaciones compacto (SEC), a través de la manipulación de estructuras de datos, lo cual mejora notablemente los métodos simbólicos tradicionales. Se demuestra que modelando todos los dispositivos activos usando nullors, el SEC se formula fácilmente por manipulación de las relaciones de interconexión del nullor y admitancias. Algunos ejemplos conducen a concluir en la confiabilidad del método simbólico propuesto para incorporarlo dentro de un simulador simbólico.
Palabras Clave: Análisis simbólico, Modelado y simulación, Teoría de circuitos, Estructura de datos, Anulador.

1 Introduction

Symbolic analysis is a powerful tool which accelerates the electronic-design process by providing insight about the behavior of a circuit [1]-[4]. Electronic design is improved by computing symbolic expressions referred as design-equations [3],[5],[6], which are quite suitable for synthesis and optimization procedures. Unfortunately, the complexity in manipulating large expressions using traditional symbolic-methods [2]-[6],[10], reduces the application to small circuits. In this manner, symbolic-methods oriented to reduce the complexity in manipulating complex symbolic expressions in large circuits, are very much needed. On one hand, the majority of the traditional symbolic-methods uses either, the modified-nodal-analysis (MNA) or the signal flow graph (SFG) techniques [2],[3],[6],[10]. However, they have the drawbacks of manipulating big matrices and complex topologies operations, respectively. On the other hand, although the Nodal Analysis (NA) method [1],[4],[9] improves the MNA and SFG ones, by modeling all active devices using nullors [7]-[11], it makes a complex matrix-reduction process by manipulating and deleting one col and one row for each nullator and norator, respectively.

To improve the computation of fully-symbolic expressions in analog circuits, this paper is focused on manipulating data structures associated to the admittances and nullor interconnection-relationships. In section 2, all active devices are modeled by nullors. A traditional NA symbolic-method is described in section 3. The proposed symbolic-method, which improves the traditional NA one, is introduced in section 4. Several examples are shown in section 5, at different levels of abstraction. Finally, the conclusions are summarized in section 6.

2 Modeling Analog Circuits

The nullor can be used to model the ideal behavior of all active devices at different levels of abstraction [2],[4],[7],[11]. In this manner, in this section all active devices are replaced by their small-signal nullor-based model, which is quite suitable to improve symbolic analysis.

2.1 Nullor Identities

The nullor can be represented as a two-port device as shown in Fig. 1(a). It is composed of two elements: the nullator connected at its input-port, where:

$$v_1 = i_1 = 0 \quad \textbf{(1)}$$

and the norator connected at its output port where:

$$v_2 = i_2 = \infty \quad \textbf{(2)}$$

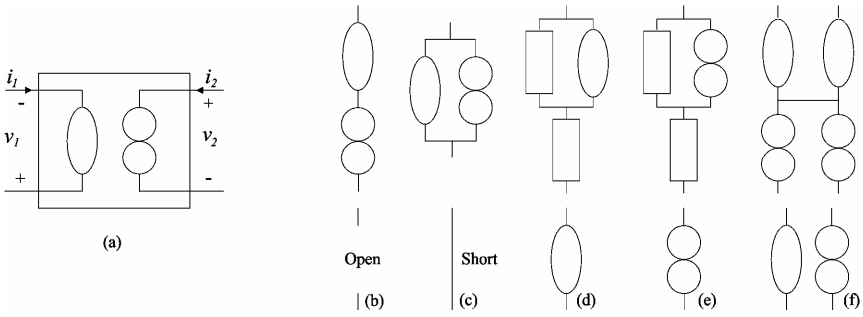

Fig. 1. (a) The nullor element, and (b)-(f) Five useful nullator-norator identities.

The nullator and norator belong to a class of elements which have no conventional matrix representation, as two-port networks, however, they are very useful in some analysis and synthesis problems by combining them appropriately, e.g. using the five identities shown in Fig. 1 [7].

2.2 The independent Voltage-source

The independent voltage-source is a non-NA-compatible element, however, using one nullor it can be modeled to be NA-compatible one, as shown in Fig. 2(a). Besides, the transformed voltage-source to a current-source adds one node and three elements more, the resulting nullor-circuit is quite appropriate to apply the NA symbolic-method than considering the independent voltage-source to apply the MNA method, as shown in section 3.

2.3 The four Controlled Sources

The four controlled sources can be modeled by applying a unified approach [1], as shown in Fig. 2. The bias references of the nullor models should be taken into account during the transformation process.

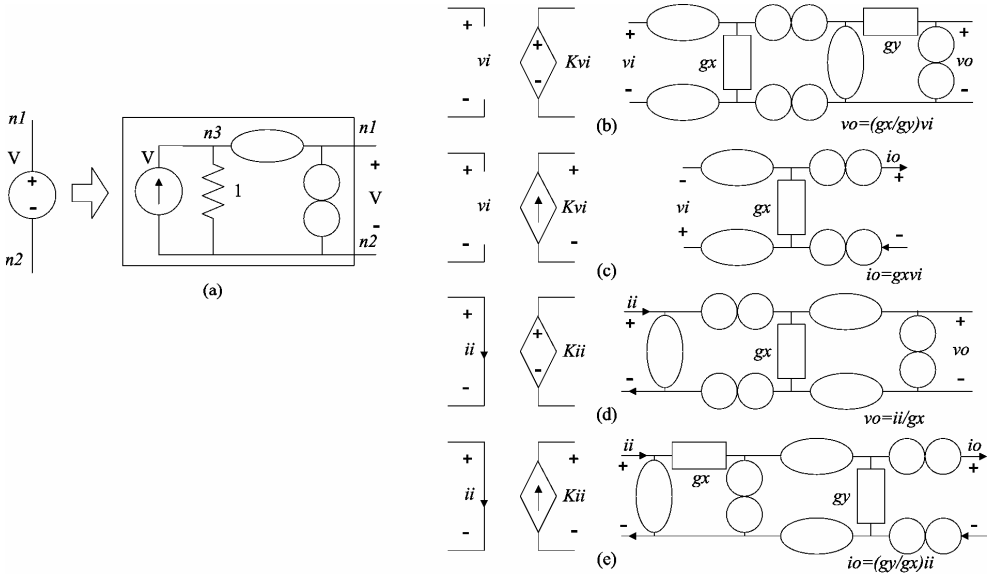

Fig. 2. (a) Transforming a voltage-source to current-source, and (b)-(e) The four controlled sources.

2.4 The Diode and Transistors

The ideal behavior of the union-diode, bipolar junction (BJT) and metal-oxide-semiconductor field-effect (MOSFET) transistors is modeled as shown in Fig. 3. A more detailed (real) model can be approximated at different levels of abstraction, e.g. the parasitic elements of a MOSFET can easily be added as shown in Fig. 3(d).

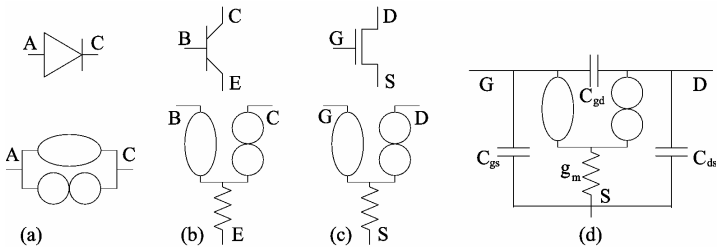

Fig. 3. (a) Ideal diode, (b) BJT, (c) MOSFET, and (d) Parasitic elements of a MOSFET.

2.5 The Opamp, OTA and CCII-

The ideal behavior of the operational amplifier (opamp) [2],[7],[11], is modeled by Fig. 4(a), where the output is always connected to ground (reference node). The operational transconductance amplifier (OTA) [8],[11],[12], is modeled by Fig. 4(b). Finally, the negative second-generation current-conveyor (CCII-) [8],[11], is modeled by Fig. 4(c).

2.6 Automatic Modeling

Any active device can be modeled as a nullor-circuit by applying the transformation process sketched in Fig. 5, where it is assumed that the initial circuit has a SPICE representation, i.e. the file *.cir.

First step: Compute the maximum node-number and, generate a data-structure containing the name, nodes and value of each circuit-element.

Second step: Transform each SPICE circuit-element using its nullor-circuit model. For example, for a MOSFET (see Fig. 3(d)), its nullor-equivalent requires the addition of a node-label between the nullor and g_m. The value of the additional node equals to the value of the (maximum node-number)+1. After modeling all circuit-elements, generate a new nullor-circuit data-structure.

Third step: The data-structure is used furtherly to formulate and solve the system of equations which models the behavior of the circuit. For noise analysis, the noise sources are added according to the model of each circuit-element [6],[9].

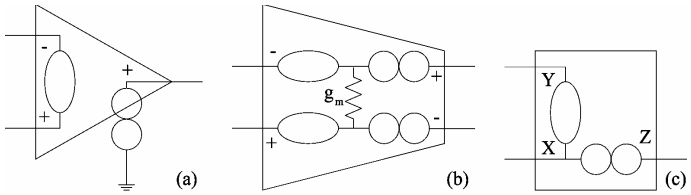

Fig. 4. (a) Opamp, (b) OTA, and (c) CCII-.

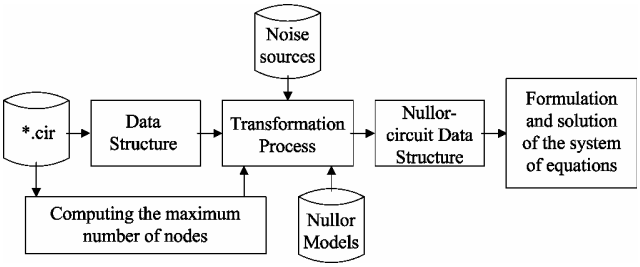

Fig. 5. Modeling SPICE circuits to nullor circuits.

3 Traditional NA Symbolic-Method

Analog modeling approaches at different levels of abstraction are quite useful and convenient to avoid time-waste if an approximated expression representing the dominant behavior of a circuit is required [1],[3],[4],[10]. That way, in section 2 it has been shown several circuit elements modeled at the most abstract level using nullors, which are useful to apply NA symbolic-methods. To describe the formulation approach of the CSEs by applying the traditional NA symbolic-method, lets consider the elliptic filter structure shown in Fig. 6 [5]. By using Fig.2(a) and Fig. 4(b), the resulting nullor circuit is shown in Fig. 7.

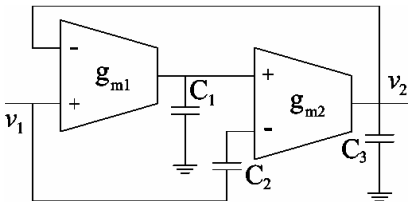

Fig. 6. OTA-based elliptic filter structure.

To compute a fully-symbolic transfer function (FSTF), the following steps should be carried out:

Step 1: Reduce to the small-signal equivalent.
Step 2: Compute (3), which has an order equal to the number of nodes (**n**).
Step 3: Compute (4), i.e. the CSEs, which has an order **m**=**n**-number of nullors.
Step 4: Compute the desired FSTF.

$$i = Y_{NA} v \tag{3}$$

$$i_{CNA} = Y_{CNA} v_{CNA} \tag{4}$$

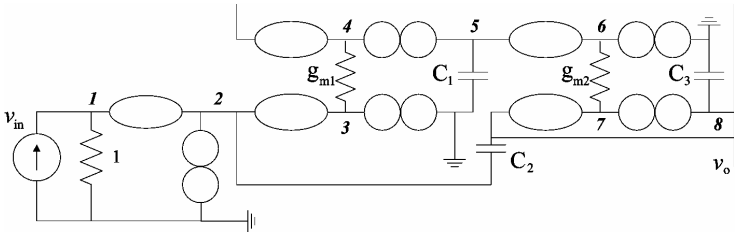

Fig. 7. Nullor equivalent of Fig. 6.

In this case, the small-signal equivalent is already given by Fig. 7. The computation of (3) is given by (5), where the elements in Y_{NA} are computed as follows:

$Y_{ij} = +\sum$ admittances connected to node $i \forall (i = j)$.

$Y_{ij} = -\sum$ admittances connected to node i and $j \forall (i \neq j)$.

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_2 & 0 & 0 & 0 & 0 & 0 & -sC_2 \\ 0 & 0 & g_{m1} & -g_{m1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -g_{m1} & g_{m1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & sC_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & g_{m2} & -g_{m2} & 0 \\ 0 & 0 & 0 & 0 & 0 & -g_{m2} & g_{m2} & 0 \\ 0 & -sC_2 & 0 & 0 & 0 & 0 & 0 & sC_2 + sC_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \end{bmatrix} \quad \textbf{(5)}$$

Equation (4) is computed by making a reduction process in (5), by applying four nullator-norator properties [4]:

(1) Delete *X*-col for a grounded-nullator (see Fig. 8(a)).
(2) Delete *X*-row for a grounded-norator (see Fig. 8(b)).
(3) For $i < j$, update $col_i = col_i + col_j$ and delete the *j*-col for a floating nullator (see Fig. 8(c)).
(4) For $i < j$, update $row_i = row_i + row_j$ and delete the *j*-row for a floating norator (see Fig. 8(d)).

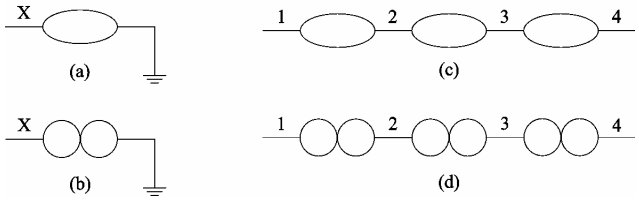

Fig. 8. (a) Grounded nullator, (b) grounded norator, (c) floating nullators, and (d) floating norators.

By applying the nullator-norator properties to (5), the CSEs is given by (6).

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -g_{m1} & g_{m1} & sC_1 \\ -sC_2 & g_{m2} + s(C_2 + C_3) & -g_{m2} \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_{4,7,8} \\ v_{5,6} \end{bmatrix} \quad \textbf{(6)}$$

Solving for the output variable, v_8 is given by (7), and finally, the FSTF is given by (8) [5]:

$$v_{4,7,8} = \frac{-v_{in}\left(g_{m1}g_{m2} + s^2C_1C_2\right)}{-g_{m1}g_{m2} - sC_1\left[g_{m2} + s(C_2 + C_3)\right]} \quad \textbf{(7)}$$

$$\frac{v_o(s)}{v_{in}(s)} = \left(\frac{C_2}{C_2 + C_3}\right) \frac{s^2 + \dfrac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\dfrac{g_{m2}}{C_2 + C_3} + \dfrac{g_{m1}g_{m2}}{C_1(C_2 + C_3)}} \tag{8}$$

As one sees, the matrix Y_{NA} in (5) has an order 8×8, which is compacted to (6), where the matrix Y_{CNA} has an order 3×*3*. So that, 55 elements were manipulated and deleted!. Cols (1,2,3), (4,7,8), and (5,6) were added and the result put in cols (1), (4), and (5), respectively, in order to delete cols (2,3,7,8,6). Rows (4,5) and (7,8) were added which results were put in rows (4) and (7), respectively, to delete rows (2,3,5,6,8).

4 Proposed NA Symbolic-Method

Compared to the traditional NA symbolic-method, this work is devoted to improve the formulation process by avoiding the computation of (3), and computing directly (4). The improvement process is done by simply manipulating data-structures [13]. The proposed method can be summarized as follows:

Step 1: Reduce the analog circuit to its small-signal equivalent.
Step 2: Compute the data-structure of the admittances, norators and nullators.
Step 3: Compute the norators and nullators interconnection-relationships (row and column variables (indexes)).
Step 4: Evaluate the cartesian product of the indexes to compute the elements in the matrix Y_{CNA}, having an order equal to **m**.
Step 5: Compute the CSEs by searching each pair of nodes (indexes) from the admittances data-structure.
Step 6: Compute the desired FSTF.

By considering the OTA-based circuit shown in Fig. 6, the proposed method is applied as follows:

Step 1: Fig. 9 shows the small-signal nullor circuit, which is represented by the netlist shown in Table 1.

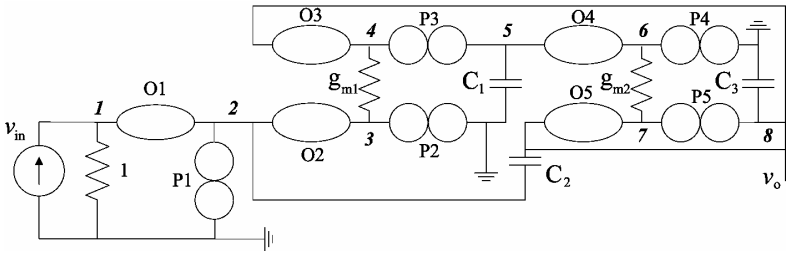

Fig. 9. Nullor circuit from Fig. 6, labeling nullator-norator pairs.

Table 1. Netlist description of Fig. 9.

Element	Nodes	Value
vin	1,0	1
N1	2,0 1,2	
N2	3,0 3,2	
N3	5,4 8,4	
N4	6,0 5,6	
N5	7,8 8,7	
1	1,0	1
gm1	4,3	
gm2	6,7	
C1	5,0	
C2	2,8	
C3	8,0	
End		

Step 2: The data-structures of the admittances, norators and nullators, are shown in Tables 2 and 3 [13]. The data-structure of the admittances elements is computed by considering that each pair of nodes (*i*,*j*), is related to two basic rules: The resulting element $Y_{(i,j)}$ is positive $\forall(i = j)$, else, it is negative $\forall(i \neq j)$.

Table 2. Data-structure of admittances.

Node 1	Node 2	Admittance
1	1	1
3	4	-gm1
3	3	gm1
4	4	gm1
6	7	-gm2
6	6	gm2
7	7	gm2
5	5	sC1
2	8	-sC2
2	2	sC2
8	8	s(C2+C3)

Table 3. Data-structure of norators and nullators.

Node 1	Node 2	Norator	Node 1	Node 2	Nullator
2	0	P1	1	2	O1
3	0	P2	3	2	O2
5	4	P3	8	4	O3
6	0	P4	5	6	O4
7	8	P5	8	7	O5

Step 3: The computation of the row and column indexes, is done according to Table 3. From rules shown in Fig. 8, the connection of norators P1, P2, and P4 indicates deletion of rows 2, 3, and 6, respectively, while norators P3 and P5, indicates an addition of rows (4,5) and (7,8), respectively. So that, the indexes associated to rows are: [(1),(4,5),(7,8)]. On the other hand, the connection of nullators (O1,O2), (O3,O5), and O4, indicates and addition of cols (1,2,3), (4,7,8), and (5,6), respectively. So that, the indexes associated to cols are: [(1,2,3),(4,7,8),(5,6)].

Step 4: The cartesian product of the indexes results in the following combinations of pair of nodes, to the elements in the matrix Y_{CNA} (rows×cols):

$Y_{(1,1)}$=(1,1)+(1,2)+(1,3), $Y_{(1,2)}$=(1,4)+(1,7)+(1,8), $Y_{(1,3)}$=(1,5)+(1,6).
$Y_{(2,1)}$=(4,1)+(4,2)+(4,3)+(5,1)+(5,2)+(5,3), $Y_{(2,2)}$=(4,4)+(4,7)+(4,8)+(5,4)+(5,7)+(5,8), $Y_{(2,3)}$=(4,5)+(4,6)+(5,5)+(5,6).
$Y_{(3,1)}$=(7,1)+(7,2)+(7,3)+(8,1)+(8,2)+(8,3), $Y_{(3,2)}$=(7,4)+(7,7)+(7,8)+(8,4)+(8,7)+(8,8), $Y_{(3,3)}$=(7,5)+(7,6)+(8,5)+ (8,6).

Step 5: By searching the admittances located at each pair of nodes (indexes) from Table 2, the resulting elements become:

$Y_{(1,1)}$=1+0+0, $Y_{(1,2)}$=0+0+0, $Y_{(1,3)}$=0+0.
$Y_{(2,1)}$=0+0-g_{m1}+0+0+0, $Y_{(2,2)}$=g_{m1}+0+0+0+0+0, $Y_{(2,3)}$=0+0+sC_1+0.
$Y_{(3,1)}$=0+0+0+0-sC_2+0, $Y_{(3,2)}$=0+g_{m2}+0+0+0+$s(C_2+C_3)$, $Y_{(3,3)}$=0-g_{m2}+0+0.

It should be pointed out that (*i*,*j*)=(*j*,*i*), and it should be considered one time if repeated in each $Y_{(i,j)}$. Finally, the resulting CSEs is given as already shown by (6).

Step 6: By computing $v_o(s)=v_{4,7,8}$, and after some symbolic-manipulations, the resulting FSTF is shown by (8). As one sees, this novel method avoids the computation of (3), which is time-consuming. Basically, the CSEs is formulated by fill-in the compact nodal-admittance matrix Y_{CNA} [4], by using the nullor interconnection-properties.

5 Examples

This section is focused on computing FSTFs of analog circuits modeled by nullors. In each example, the formulation of the CSEs is done by applying the proposed symbolic-method given in section 4. The solution to compute the FSTF is done by applying Cramer's rule.

5.1 Opamp Circuits

Lets consider the generalized impedance converter (GIC) implemented with two opamps [2], as shown in Fig. 10(a). Its nullor representation, using Fig. 4(a), is shown in Fig. 10(b), where the CSEs has an order **m**=5nodes-2nullors=3.

The rows and cols variables (indexes) are: [(1),(3),(5)] and [(1,3,5),(2),(4)], respectively. After computing the cartesian product, the CSEs is given by (9). The resulting input-impedance becomes equal to (10).

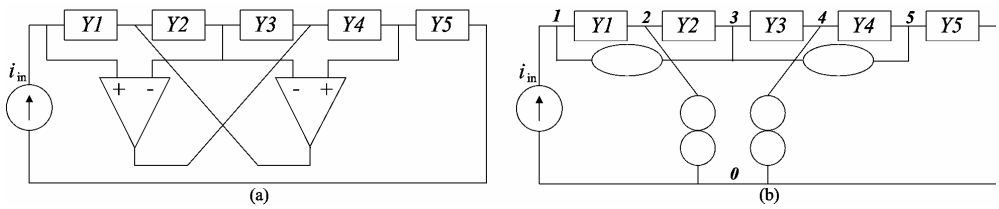

Fig. 10. (a) GIC implemented with opamps, and (b) Its nullor-equivalent circuit.

$$\begin{bmatrix} i_{in} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Y_1 & -Y_1 & 0 \\ Y_2+Y_3 & -Y_2 & -Y_3 \\ Y_4+Y_5 & 0 & -Y_4 \end{bmatrix} \begin{bmatrix} v_{1,3,5} \\ v_2 \\ v_4 \end{bmatrix} \tag{9}$$

$$Z_{in} = \frac{v_{1,3,5}}{i_{in}} = \frac{Y_2 Y_4}{Y_1 Y_3 Y_5} \tag{10}$$

5.2 OTA and CCII- Circuits

A GIC implemented with two OTAs is shown in Fig. 11(a) [5],[12]. Its nullor representation, using Fig. 4(b), is shown in Fig. 11(b). The CSEs has an order **m**=6nodes-4nullors=2.

The rows and cols variables (indexes) are: [(1,4),(2,6)] and [(1,2),(5,6)], respectively. After computing the cartesian product, the CSEs is given by (11). The resulting input-impedance becomes equal to (12).

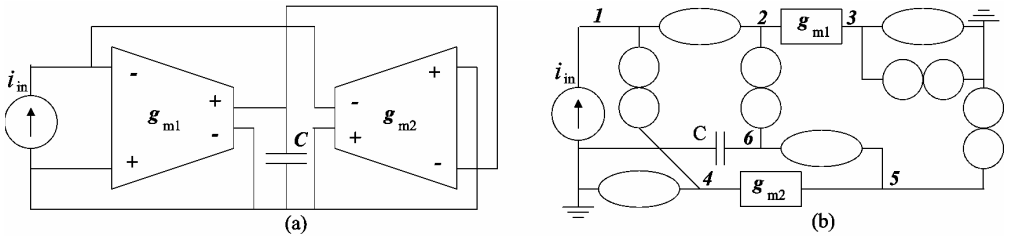

Fig. 11. (a) GIC implemented with OTAs, and (b) Its nullor-equivalent circuit.

$$\begin{bmatrix} i_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -g_{m2} \\ g_{m1} & sC \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_{5,6} \end{bmatrix} \tag{11}$$

$$Z_{in} = \frac{v_{1,2}}{i_{in}} = \frac{sC}{g_{m1} g_{m2}} \tag{12}$$

Looking to Fig. 4(c), the GIC shown in Fig. 11(b) can be synthesized by using four CCII-s [14]. The input-impedance will be the same for the GIC implemented with either two-OTAs or four-CCII-s.

5.3 CMOS circuits

For CMOS circuits, the models representing the behavior of each MOSFET can be implemented at different levels of abstraction. Lets consider the low-voltage CMOS current-amplifier circuit shown in Fig. 12(a). By modeling each MOSFET using Fig. 3(d), and by eliminating the drain-source parasitic-capacitance, the nullor circuit is shown in Fig. 12(b). The nullor circuit contains eight-nodes and four-nullors, so that the CSEs equals to order four.

The resulting row and col indexes are: [(1,8),(2,6), (3,4),(5,7)] and [(1),(2,3,8),(4),(5)]. By considering that the four MOSFETs have the same g, C_{gs}, and C_{gd}, and by eliminating C_{gd}, the CSEs is given by (13), and the final approximated FSTF is given by (14).

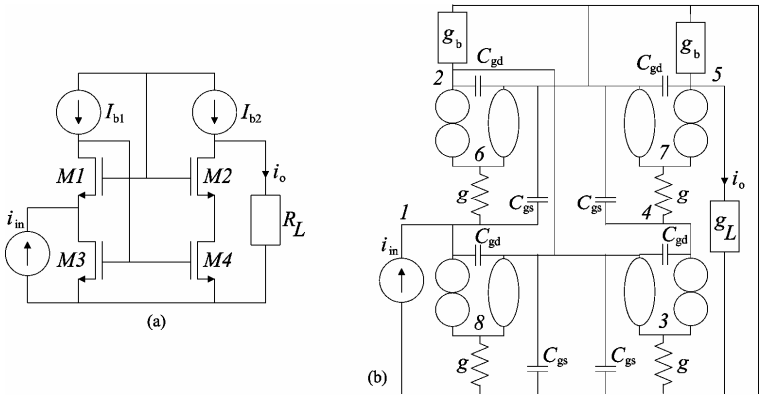

Fig. 12. (a) Low-voltage CMOS current amplifier, and (b) Its nullor-equivalent circuit.

5.4 BJT Circuits

For the BJT circuit shown in Fig. 13(a), by using the model shown in Fig. 3(b), by eliminating the transconductance, and by open-circuiting all current biases, the small-signal nullor-equivalent circuit is shown in Fig. 13(b).

$$\begin{bmatrix} i_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} g_1 + sC_{gs1} & g_1 & 0 & 0 \\ -g_1 & g_b + 2sC_{gs1} & 0 & 0 \\ 0 & g_1 & g_1 + sC_{gs1} & 0 \\ 0 & 0 & -g_1 & g_b + g_L \end{bmatrix} \begin{bmatrix} v_1 \\ v_{2,3,8} \\ v_4 \\ v_5 \end{bmatrix} \quad \textbf{(13)}$$

$$\frac{i_o(s)}{i_{in}(s)} = \frac{g^3}{2s^3C_{gs}^3 + 5gs^2C_{gs}^2 + 5g^2C_{gs} + 2g^3} \quad \textbf{(14)}$$

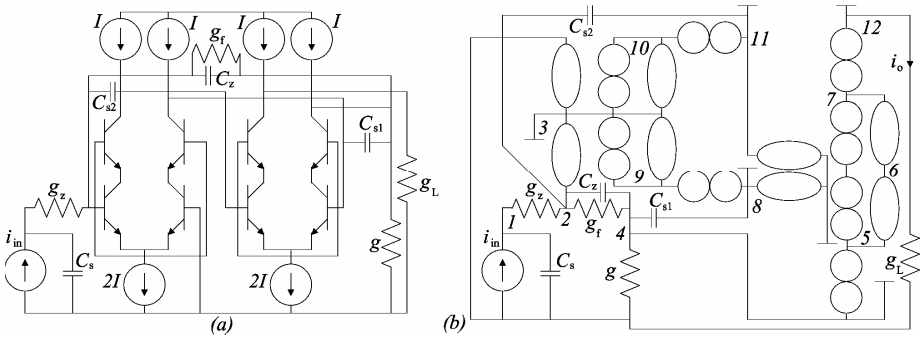

Fig. 13. (a) BJT-based current amplifier, and (b) Its nullor-equivalent circuit.

The nullor circuit contains twelve-nodes and eight-nullors, so that the CSEs equals to order four. The resulting row and col indexes are: [(1),(2),(3,8,9,10,11),(4,5,6,7,12)] and [(1),(4),(5,6,7,8,11),(12)]. The CSEs is given by (15), and the final approximated FSTF is given by (16).

$$\begin{bmatrix} i_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} g_z + sC_s & 0 & 0 & 0 \\ -g_z & -g_f - sC_z & -sC_{s2} & 0 \\ 0 & -sC_{s1} & sC_{s1} + sC_{s2} & 0 \\ 0 & g_f + g + sC_z + sC_{s1} & -sC_{s1} & g_L \end{bmatrix} \begin{bmatrix} v_1 \\ v_4 \\ v_{5,6,7,8,11} \\ v_{12} \end{bmatrix} \tag{15}$$

$$\frac{i_o(s)}{i_{in}(s)} = -\frac{g_z\left[(C_{s1}+C_{s2})(g_f+g+sC_z+sC_{s1})-sC_{s1}^2\right]}{(g_z+sC_s)\left[(g_f+sC_z)(C_{s1}+C_{s2})+sC_{s1}C_{s2}\right]} \tag{16}$$

As one sees, the proposed symbolic-method enhances the calculation of a FSTF of an analog circuit by using nullors. For large circuits, this method could be applied after the reduction of the circuit-elements, as shown in [15], where all non-dominant terms are eliminated before the formulation of the CSEs.

6 Conclusion

A novel nodal-analysis method has been introduced to compute fully-symbolic expressions in analog circuits whose behavior is modeled by using nullors. It has been shown that by manipulating data-structures, it results in a suitable symbolic-method improving complex manipulations at different levels of abstraction, i.e. at the macromodel and transistor circuit level.

The proposed symbolic-method has been based on the computation of a compact system of equations, which highly improves traditional symbolic-methods. It was demonstrated that by modeling all active devices using nullors, the CSEs is easily formulated by manipulating both the nullor and admittance interconnection-relationships. Finally, from the examples presented in section 5, one can conclude on the suitability and appropriateness of the proposed symbolic-method to be incorporated within an environment of analog design automation.

Acknowledgment

This work was supported in part by CONACyT/MEXICO under project number 40321, and CoSNET/MEXICO under project number 454.03p.

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